WHAT IS CLAIMED IS:

1. A frequency discriminator for detecting phase shifts between sequential pulses in a frequency-shift keyed (FSK) signal having a nominal frequency, f, said frequency discriminator comprising:

a first current controlled delay line capable of receiving said FSK signal and delaying said FSK signal by a desired time delay to thereby produce a time-delayed FSK signal;

a first multiplier capable of receiving and multiplying said FSK signal and said time-delayed FSK signal to thereby produce an output product signal proportional to a phase shift between said FSK signal and said time-delayed FSK signal; and

a delay locked loop comprising a second current controlled delay line substantially similar to said first current controlled delay line, wherein said delay locked loop receives a reference clock signal having a time period equal to said desired time delay and adjusts a control current level in said second current controlled delay line until a delay of said second current controlled delay line matches said time period of said reference clock signal, wherein said control current level is then used to adjust a delay of said first current controlled delay line.

2. The frequency discriminator as set forth in Claim 1 wherein said delay locked loop adjusts said control current level of said second current controlled delay line by adjusting a bias current in said second current controlled delay line.

3. The frequency discriminator as set forth in Claim 2 wherein said delay locked loop adjusts said delay of said first current controlled delay line by adjusting a bias current in said first current controlled delay line to match said bias current in said second current controlled delay line.

4. The frequency discriminator as set forth in Claim 3 wherein said delay locked loop comprises a phase detector having a first input for receiving said reference clock signal and a second input for receiving an output signal of said second current controlled delay line and generating a correction control signal determined by a phase difference between said reference clock signal and said output signal of said second current controlled delay line.

5. The frequency discriminator as set forth in Claim 4 wherein said second current controlled delay line is configured as an oscillator.

6. The frequency discriminator as set forth in Claim 2 further comprising:

a third current controlled delay line capable of receiving said FSK signal and delaying said FSK signal by a desired time delay to thereby produce a time-delayed FSK signal; and

a second multiplier capable of receiving and multiplying said FSK signal and said time-delayed FSK signal to thereby produce an output product signal proportional to a phase shift between said FSK signal and said time-delayed FSK signal; wherein said delay locked loop uses said control current level to adjust a delay of said third current controlled delay line.

7. The frequency discriminator as set forth in Claim 6 wherein said delay locked loop adjusts said delay of said third current controlled delay line by adjusting a bias current in said third current controlled delay line to match said bias current in said second current controlled delay line.

8. A frequency-shift keyed (FSK) receiver comprising:

demodulation circuitry capable of receiving an incoming radio frequency (RF) signal and generating therefrom a frequency-shift keyed (FSK) signal having a nominal frequency, f,; and

a frequency discriminator coupled to said demodulation circuitry for detecting phase shifts between sequential pulses in said FSK signal, said frequency discriminator comprising:

a first current controlled delay line capable of receiving said FSK signal and delaying said FSK signal by a desired time delay to thereby produce a time-delayed FSK signal;

a multiplier capable of receiving and multiplying said FSK signal and said time-delayed FSK signal to thereby produce an output product signal proportional to a phase shift between said FSK signal and said time-delayed FSK signal; and

a delay locked loop comprising a second current controlled delay line substantially similar to said first current controlled delay line, wherein said delay locked loop receives a reference clock signal having a time period equal to said desired time delay and adjusts a control current level in said second current controlled delay line until a delay of said second current controlled delay line matches said time period of said reference clock signal, wherein said control current level is then used to adjust a

delay of said first current controlled delay line.

9. The frequency-shift keyed receiver as set forth in Claim 8 wherein said delay locked loop adjusts said control current level of said second current controlled delay line by adjusting a bias current in said second current controlled delay line.

10. The frequency-shift keyed receiver as set forth in Claim 9 wherein said delay locked loop adjusts said delay of said first current controlled delay line by adjusting a bias current in said first current controlled delay line to match said bias current in said second current controlled delay line.

11. The frequency-shift keyed receiver as set forth in Claim 10 wherein said delay locked loop comprises a phase detector having a first input for receiving said reference clock signal and a second input for receiving an output signal of said second current controlled delay line and generating a correction control signal determined by a phase difference between said reference clock signal and said output signal of said second current controlled delay line.

12. The frequency-shift keyed receiver as set forth in Claim 11 wherein said second current controlled delay line is configured as an oscillator.

13. The frequency-shift keyed receiver as set forth in Claim 9 further comprising:

a third current controlled delay line capable of receiving said FSK signal and delaying said FSK signal by a desired time delay to thereby produce a time-delayed FSK signal; and

a second multiplier capable of receiving and multiplying said FSK signal and said time-delayed FSK signal to thereby produce an output product signal proportional to a phase shift between said FSK signal and said time-delayed FSK signal; wherein said delay locked loop uses said control current level to adjust a delay of said third current controlled delay line.

14. The frequency-shift keyed receiver as set forth in Claim 13 wherein said delay locked loop adjusts said delay of said third current controlled delay line by adjusting a bias current in said third current controlled delay line to match said bias current in said second current controlled delay line.

15. A method of controlling a frequency discriminator operable to detect phase shifts between sequential pulses in a frequency-shift keyed (FSK) signal having a nominal frequency, f, the method comprising the steps of:

in a first current controlled delay line, delaying the FSK signal by a desired time delay to thereby produce a time-delayed FSK signal;

in a multiplier, multiplying the FSK signal and the time-delayed FSK signal to thereby produce an output product signal proportional to a phase shift between said FSK signal and said time-delayed FSK signal;

in a delay locked loop comprising a second current controlled delay line substantially similar to the first current controlled delay line, receiving a reference clock signal having a time period equal to the desired time delay and adjusting a control current level in the second current controlled delay line until a delay of the second current controlled delay line matches the time period of the reference clock signal; and

adjusting a delay of the first current controlled delay line according to the control current level.

16. The method as set forth in Claim 15 wherein the step of adjusting the control current level of the second current controlled delay line comprises the step of adjusting a bias current in the second current controlled delay line.

17. The method as set forth in Claim 16 wherein the step of adjusting the delay of the first current controlled delay line comprises the step of adjusting a bias current in the first current controlled delay line to match the bias current in the second current controlled delay line.

18. The method as set forth in Claim 17 wherein the delay locked loop comprises a phase detector having a first input for receiving the reference clock signal and a second input for receiving an output signal of the second current controlled delay line and generating a correction control signal determined by a phase difference between the reference clock signal and the output signal of the second current controlled delay line.

19. The method as set forth in Claim 18 wherein the second current controlled delay line is configured as an oscillator.

20. The method as set forth in Claim 16 further comprising the steps of:

in a third current controlled delay line, delaying the FSK signal by a desired time delay to thereby produce a time-delayed FSK signal;

in a second multiplier, multiplying the FSK signal and the time-delayed FSK signal to thereby produce an output product signal proportional to a phase shift between said FSK signal and said time-delayed FSK signal; and

adjusting a delay of the third current controlled delay line according to the control current level.

21. The method as set forth in Claim 20 wherein the step of adjusting the delay of the third current controlled delay line comprises the step of adjusting a bias current in the third current controlled delay line to match the bias current in the second current controlled delay line.